Addressing Power Issues in Real Time Clock Applications

Introduction

Intersil Real Time Clock (RTC) products now include many products with a variety of functions. Common functions include a low power 32,768kHz oscillator and also the ability to keep time in SRAM registers after initial time and date is set.

The power for RTC devices includes a V_{DD} source, and can also include a backup source of either a battery or large storage capacitor (super capacitor). In many applications the RTC device is the only device in a system that has an alternative power source such as the backup battery, so there can be unique demands placed on the device compared to other semiconductor products.

In addition, the RTC device has a communications bus, usually I^2C, that has pull-up resistors which can go to a different power source than the RTC. The interrupt or frequency output pull-up can be connected to yet another voltage.

Some RTC devices contain non-volatile EEPROM storage, both for device control registers and for general purpose storage. The EEPROM is a robust storage method that can survive temperature extremes, millions of write cycles and up to 10 years of endurance. Despite the robust design, there are power and ground voltage transients that, although they exceed data sheet limits, are present in systems and may upset EEPROM memory cells. In addition, some applications may have I^2C communication during power-down, another possible source of upset.

RTC Device Power Connections

The typical applications circuit for the RTC is shown in Figure 1. This seemingly simple circuit has no less than 4 possible power connections:

- V_{DD} power (V_{POWER})
- I^2C bus open drain pull-up power (V_{BUS})
- Battery backup (V_{BAT})
- Frequency output or interrupt open drain pull-up (V_{FOUT})

Having four different power sources raises the issue of power sequencing. Ideally, the RTC circuit will have 3 of the four power sources in common. The V_{CC}, V_{BUS} and V_{FOUT} should all connect to the main V_{POWER} source, and when that is the case there are virtually no concerns with power sequencing.

Many applications prefer to have these connections powered separately. Examples include:

- RTC device is powered down while the I^2C bus and microcontroller are active (not recommended since it will violate RTC data sheet, but RTC devices are OK in this state).
- RTC device is powered down while the F_{OUT} or $\overline{IRQ}$ is pulled up to V_{BAT} to allow a wake-up interrupt or clock while other circuits are asleep (this is OK, but the RTC data sheet absolute maximum ratings need to be followed).
- RTC device is powered from a higher or lower voltage than the I^2C pull-ups (this may or may not be allowed, possible unreliable operation).
- RTC device operates with one supply voltage and the V_{BAT} pin is grounded (this is OK, and is covered later in this document).

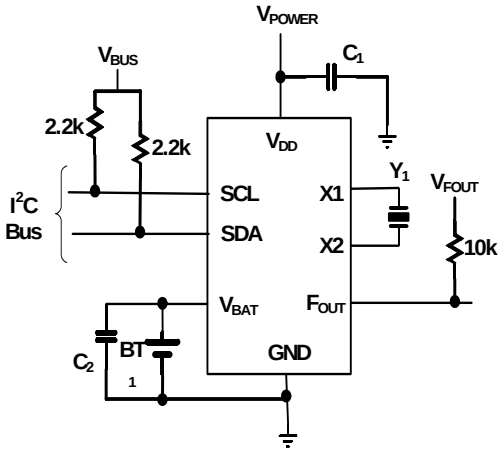

FIGURE 1. TYPICAL RTC APPLICATION CIRCUIT

Table 1 provides some guidance when designing an RTC applications circuit.

TABLE 1. RTC POWER CONNECTION GUIDELINES

	DESCRIPTION	V_{DD}	SCL	SDA	F_{OUT} / $\overline{IRQ}$	V_{BAT}	COMMENT
1	Normal Operation, 5V	5V	5V	5V	5V	<5.0V	All pull-ups same source as V_{DD}. No Issues. OK if V_{BAT} is a super capacitor.
2	Normal Operation, 3.3V	3.3V	3.3V	3.3V	3.3V	**<3.6V**	OK. Normally V_{BAT} up to 5.5V (super capacitor) is OK. Check applicable data sheet.
3	Split Supplies, Low Voltage Four/IRQ-	5V	5V	5V	3.3V	<5.0V	OK. The F_{OUT} can connect to 3.3V circuits reliably.
4	Split Supplies, Lower Voltage I^2C (a)	5V	**3.3V**	**3.3V**	5V or 3.3V	<5.0V	**Will not work.** The V_{IH} for the I^2C is based on V_{DD} and prevents communications.
5	Split Supplies, Lower Voltage I^2C (b)	5V	**V_{BAT}**	**V_{BAT}**	5V or 3.3V	<3.5V	**Will not work.** The V_{IH} for the I^2C is based on V_{DD} and prevents communications, especially as V_{BAT} discharges. V_{BAT} discharges quickly too.
6	Split Supplies, High Voltage V_{BAT}, Variable Voltage I^2C	**3.3V**	**V_{BAT}**	**V_{BAT}**	3.3V	<5.0V	Will work on **SOME** RTC's. Be careful for $V_{BAT} > V_{DD}$ as the device may not access I^2C in this mode or can draw high V_{BAT} current. Check applicable data sheet. Note that with V_{BAT} discharging to 2.0V or below, the V_{IH} will be too low for V_{DD}-referenced I^2C. V_{BAT} discharges quickly too.
7	Split Supplies, Low voltage V_{BAT}, Variable Voltage I^2C	**3.3V**	**V_{BAT}**	**V_{BAT}**	3.3V	<V_{DD}	Will work on **MOST** RTC's. Check applicable data sheet. Note that with V_{BAT} discharging to 2.0V or below, the V_{IH} will be too low for V_{DD}-referenced I^2C. V_{BAT} discharges quickly too.
8	Split Supplies, Higher Voltage I^2C	3.3V	**5.0V**	**5.0V**	3.3V	<5.0V	Will work on all RTC devices but **NOT ADVISED**. Potential for latch-up and high V_{BAT} current exists, some RTC may have issues. Follow absolute maximum ratings on data sheet.
9	Split Supplies F_{OUT} has One Supply and V_{DD} another, Low Voltage V_{DD}	**3.3V**	**3.3V**	**3.3V**	5V or 3.3V	3.0V to 5.0V	Will work on all RTC devices but not advised. If unavoidable, make sure to apply both supplies at close to the same time.

NOTE: Consult data sheet for RTC V_{DD} operation below 2.7V.

Powering the RTC ON and OFF

Most Intersil RTC devices contain an internal power switch that applies the battery power to the internal circuitry when the V_{DD} voltage drops below a certain threshold. That threshold is generally selectable, depending on the device (see applicable data sheet).

Since the RTC device is very low power, the switch circuitry is fairly slow, and can take more than 50µs to completely switch to the battery voltage. If the V_{DD} power-down ramp is faster than this time, the internal RAM registers may not have sufficient voltage to retain their values and may become corrupted or reset altogether.

If a V_{DD} power source needs to power-down quickly for some reason, the RTC should have some extra capacitance at the V_{DD} pin to slow down the ramp to >50µs. If the extra capacitance is not realistic, then a small series resistor can be added to form an R-C network which will give the RTC a dedicated power-down and power-up waveform. Since the supply current for RTC's can go up to 1mA or 2mA during write functions (if EEPROM is included), then it's a good idea to use about a 100Ω resistor to keep the maximum drop reasonable.

Power Supply Turn-On Issues

Some applications involving the RTC device may unknowingly expose the device to excessive transients which may not permanently damage the device, but may corrupt the EEPROM and SRAM contents. Specifically, those applications which use offline AC power and switch it on and off can produce voltage bounces on the ground or V_{DD}, or both, with enough energy and fast enough speed to propagate across a PC board despite bulk and decoupling capacitance at supply pins. In some cases, the energy supplied and the resulting current pulse is so large and fast that high intensity spikes can occur, capable of producing voltages exceeding the absolute maximum for IC's. For negative pulses, the internal ESD diodes can absorb this energy but are limited, and the resulting negative excursion can be many volts, triggering latch-up or disruptive events. The RTC device can be uniquely susceptible to this bounce since it has a battery input and is expected to retain proper data in the SRAM through power turn-on and turn-off. In cases where the battery input is grounded, a device with EEPROM can have the data bits corrupted. It requires a large amount of energy to do this, with device currents and voltages that exceed the absolute maximum ratings.

The worst case scenario is where the AC waveform is near its peak during turn-on and the board instantly sees that peak before passive devices absorb the energy.

Normal power supply filtering does help prevent this, and adding small amounts of inductance can improve it or make it worse, depending on the location of the inductance and decoupling capacitance. The best prevention is to add a medium power Schottky diode at the RTC, anode at ground and cathode at V_{DD}, which can clamp the voltage across the device to a safe value at higher currents than the internal ESD structures. A good low leakage diode such as the BAT54 is recommended.

Power Glitches or Interruptions

The battery backup design for RTC's is there to insure the device retains the time/date in the event the power is turned off or interrupted for some reason. Battery backup works fine for most applications where the power is turned off and on predictably.

Occasions arise where there may be fast glitches or excursions of the V_{DD} beyond the absolute maximum limits, and these will cause problems. If a fast glitch is generated by power switching or interruption, then RAM contents can be corrupted or reset (see section "Powering the RTC ON and OFF" on page 2). Again, local filtering of the V_{DD} may be needed to prevent memory corruption.

Many Intersil RTC devices contain a power-up delay function to prevent accidental access by the serial bus before power is stable and devices on a board are functioning properly. This delay is normally about 90ms, and some older devices may have a 3 second delay. After the glitch or power-up, the delay is triggered and the device will not respond to an I^2C communication until the timeout period is over. If a customer is unsure about this function in their application, they should contact Intersil.

Powering the RTC with NO or VERY LOW V_{BAT}

RTC device operation relies on stable contents in the internal registers. These SRAM registers get loaded with values either from EEPROM or default hard-coded values on power-up, depending on the RTC device type. There are two circuit configurations which lend themselves to corruption of the SRAM registers:

1. The V_{BAT} pin is grounded

In this case there is just a main V_{DD} power source which may power-down occasionally. If this voltage is allowed to float to a non-zero state on power-down, the ensuing power-up may put the SRAM registers in an unknown state.

Practical tests have shown that the SRAM registers can maintain their contents down to V_{DD} = 1.0V at room temperature. Once V_{DD} drops to <0.2V and then rises to its normal level, then the default values will be loaded. With V_{DD} stalled in the range from 0.2V to 1.0V (the "High Risk" range) on power-down, the SRAM registers can be in an unknown value on power-up.

Note that the V_{DD} power glitch to this lower voltage for a period of time can also trigger the SRAM corruption. If the glitch is not recognized by the rest of the system the RTC device can lose SRAM bits without notice. Practical tests show that the glitch would need to be minimum 50µs to 100µs duration to cause a problem.

A solution for corrupted RTC SRAM on power-up is to add a series resistor and clamp MOSFET to the RTC V_{DD} as shown in Figure 2.

Applying a logic high to the RTC_SD node (M_1 gate) will cause M_1 to saturate and discharge C_1 while pulling current through R_S. This action clamps the V_{RTC} node (V_{DD}) low, to around 20mV-30mV or less. When the logic signal is released, C_1 will charge up through R_S and V_{DD} will be powered up normally, with registers in the correct default or EEPROM recalled states. R_S must be chosen so that there enough headroom for the RTC to operate at maximum V_{DD} current, which is normally for an I^2C write. RTC devices containing EEPROM will draw more current, about 1mA during write operations and will need a smaller R_S value.

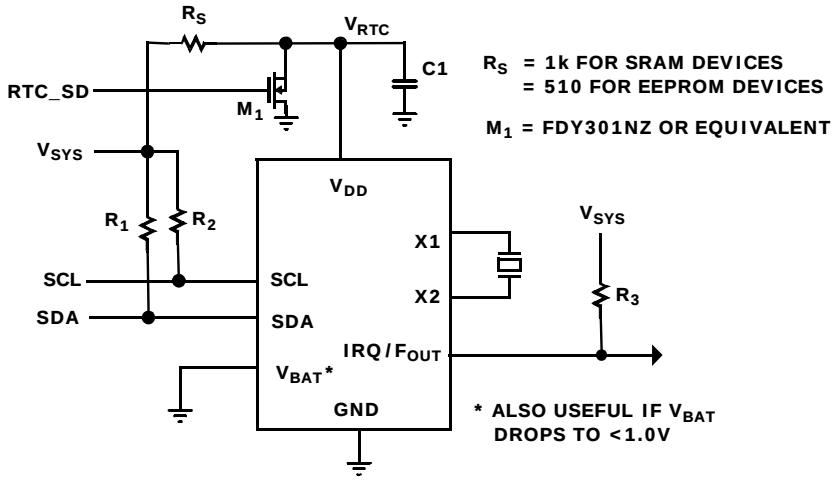

FIGURE 2. POWERING A DEVICE WITH NO BATTERY BACKUP

A secondary benefit of the R_S-C_1 circuit is filtering glitches, preventing unwanted noise on the V_{DD} pin. Note that the SDA, SCL and IRQ/F_{OUT} pins all are powered through pull-ups during the V_{DD} power cycle. This state is allowed short term and will not harm the device.

2. V_{BAT} is allowed to drop into the high risk range

In this case, the backup supply may discharge to a very low voltage (0.2V < V_{BAT} < 1V is considered very unreliable for backup power, as well). Now the RTC device is relying on V_{BAT} bias to power the SRAM registers and maintain their contents. When the V_{BAT} level drops to a low voltage, but not zero, it may be too low to maintain the SRAM bits and once V_{DD} power is cycled, they will either corrupt the current contents or incorrectly recall the default or EEPROM settings. Unless the system monitors the battery voltage, it will assume all RTC functions are normal.

If the system can detect bad data from the RTC or low V_{BAT} has been detected, then the battery should be replaced and the device should restore original SRAM register settings before operation proceeds.

The circuit from Figure 3 can be used with the jumper J_{BAT} for manually disconnecting the battery to allow the device to reset if the battery or super capacitor is discharged. Once the battery is changed or the super capacitor is charged again, the jumper can be replaced.

I²C Communication During Power-Down

Most systems will have an orderly power-down sequence, including completing I²C communications before complete power voltage shutdown. If that is not possible, then I²C communication during battery switchover can occur which may result in erroneous register writes. These register writes could result in incorrect data being written to a valid address, or having correct data written to an incorrect address. Either way, the erroneous write could change data in EEPROM (if it exists) or battery backed SRAM. Erroneous data in RTC control registers can result in the device not operating properly, even preventing I²C communication with V_{DD} powered up.

Steps should be taken to prevent any I²C activity during V_{DD} power-down situations.

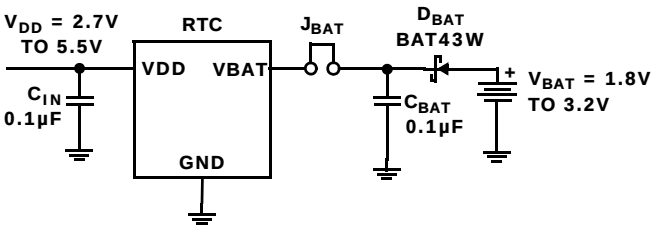

FIGURE 3. SUGGESTED BATTERY-BACKUP CIRCUIT

Conclusions

Intersil RTC devices are designed to provide a reliable clock and calendar function with battery backed up data in registers. There are some power supply situations that need to be considered in order to maintain reliable data and also serial bus communication. With these considerations, RTC applications can be made reliable and robust.